



OPA2107

Precision Dual *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: $8\text{nV}/\sqrt{\text{Hz}}$ at 10kHz
- LOW V_{os} : 500 μV max
- LOW DRIFT: 5 $\mu\text{V}/^\circ\text{C}$ max
- LOW I_B : 5pA max
- FAST SETTLING TIME: 2 μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

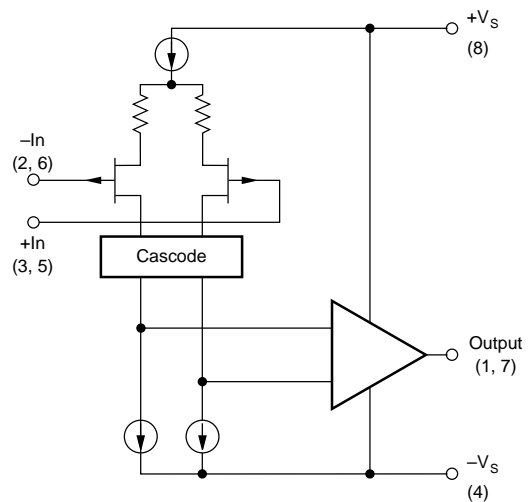
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision *Difet* performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET[®] type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (*Difet*) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP, metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.



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BIFET[®] National Semiconductor

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SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA2107AM, SM, AP, AU			OPA2107BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Over Specified Temperature SM Grade Average Drift Over Specified Temperature Power Supply Rejection	V _{CM} = 0V V _S = ±10 to ±18V		100 0.5 0.8 3	1mV 2 2.5 10		50 0.2 2	500 1 5	μV mV mV μV/°C dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Over Specified Temperature SM Grade Input Offset Current Over Specified Temperature SM Grade	V _{CM} = 0V V _{CM} = 0V		4 0.25 4 1 1	10 1.5 35 8 1 28		2 0.15 0.5	5 1 3 0.5	pA nA nA pA nA nA
INPUT NOISE Voltage: f = 10Hz f = 100Hz f = 1kHz f = 10kHz BW = 0.1 to 10Hz BW = 10 to 10kHz Current: f = 0.1Hz thru 20kHz BW = 0.1Hz to 10Hz	R _S = 0		30 12 9 8 1.2 0.85 1.2 23			* * * * * * 0.9 17		nV/√Hz nV/√Hz nV/√Hz nV/√Hz μVp-p μVrms fA/√Hz fAp-p
INPUT IMPEDANCE Differential Common-Mode			10 ¹³ 2 10 ¹⁴ 4			* *		Ω pF Ω pF
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature SM Grade Common-Mode Rejection	V _{CM} = ±10V	±10.5 ±10.2 ±10 80	±11 ±10.5 ±10.3 94		* * 84	* * 100		V V V dB
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature SM Grade	V _O = ±10V, R _L = 2kΩ	82 80 80	96 94 92		84 82	100 96		dB dB dB
DYNAMIC RESPONSE Slew Rate Settling Time: 0.1% 0.01% Gain-Bandwidth Product THD + Noise Channel Separation	G = +1 G = -1, 10V Step G = 100 G = +1, f = 1kHz f = 100Hz, R _L = 2kΩ	13	18 1.5 2 4.5 0.001 120		* * * * * *	* * * * * *		V/μs μs μs MHz % dB
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		±4.5	±15 ±4.5	±18 ±5	* *	* *	* *	V V mA
OUTPUT Voltage Output Over Specified Temperature SM Grade Short Circuit Current Output Resistance, Open-Loop Capacitive Load Stability	R _L = 2kΩ 1MHz G = +1	±11 ±10.5 ±10.2 ±10	±12 ±11.5 ±11.3 ±40 70 1000		* * * * * *	* * * * * *		V V V mA Ω pF
TEMPERATURE RANGE Specification AP, AU, AM, BM SM Operating AP, AU AM, BM, SM Storage AP, AU AM, BM, SM Thermal Resistance (θ _{J-A}) AP AU AM, BM, SM		-25 -55 -25 -55 -40 -65		+85 +125 +85 +125 +125 +150	* * * * *		* *	°C °C °C °C °C °C °C/W °C/W °C/W

* Specifications same as OPA2107AM. NOTE: (1) Specified with devices fully warmed up.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18V$
Input Voltage Range	$\pm V_S \pm 2V$
Differential Input Voltage	Total $V_S \pm 4V$
Operating Temperature	
M Package	$-55^{\circ}C$ to $+125^{\circ}C$
P and U Packages	$-25^{\circ}C$ to $+85^{\circ}C$
Storage Temperature	
M Package	$-65^{\circ}C$ to $+150^{\circ}C$
P and U Packages	$-40^{\circ}C$ to $+125^{\circ}C$
Output Short Circuit to Ground ($T_A = +25^{\circ}C$)	Continuous
Junction Temperature	$+175^{\circ}C$
Lead Temperature	
M and P Packages (soldering, 10s)	$+300^{\circ}C$
U Package, SOIC (3s)	$+260^{\circ}C$

PACKAGE INFORMATION

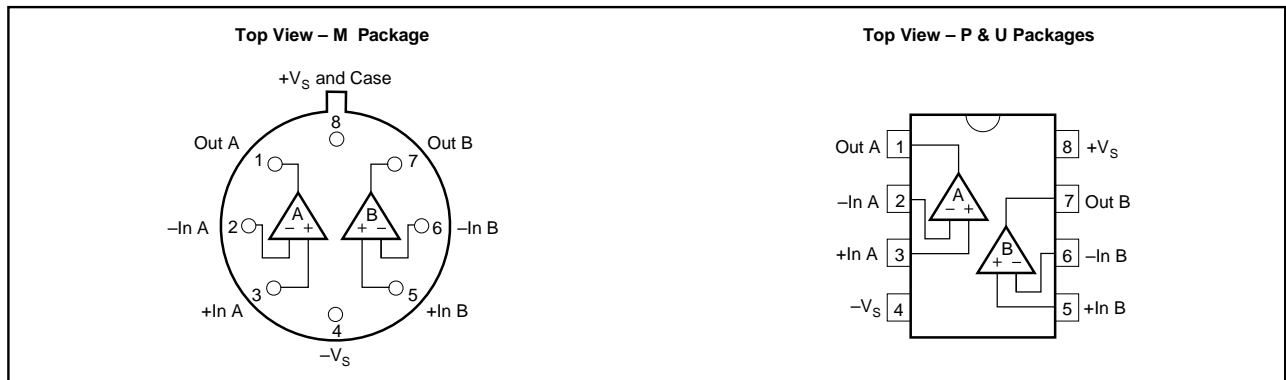
MODELS	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA2107AP	Plastic DIP	006
OPA2107AM	Metal TO-99	001
OPA2107BM	Metal TO-99	001
OPA2107SM	Metal TO-99	001
OPA2107AU	SO-8 SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODELS	PACKAGE	SPECIFICATION TEMPERATURE RANGE
OPA2107AP	Plastic DIP	-25 to $+85^{\circ}C$
OPA2107AM	Metal TO-99	-25 to $+85^{\circ}C$
OPA2107BM	Metal TO-99	-25 to $+85^{\circ}C$
OPA2107SM	Metal TO-99	-55 to $+125^{\circ}C$
OPA2107AU	SO-8 SOIC	-25 to $+85^{\circ}C$

PIN CONFIGURATIONS



DICE INFORMATION

OPA2107 DIE TOPOGRAPHY

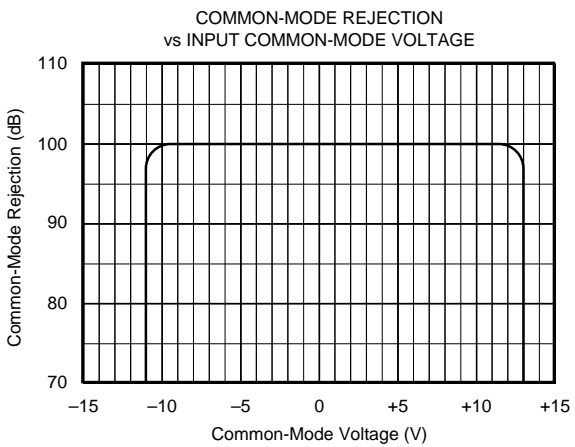
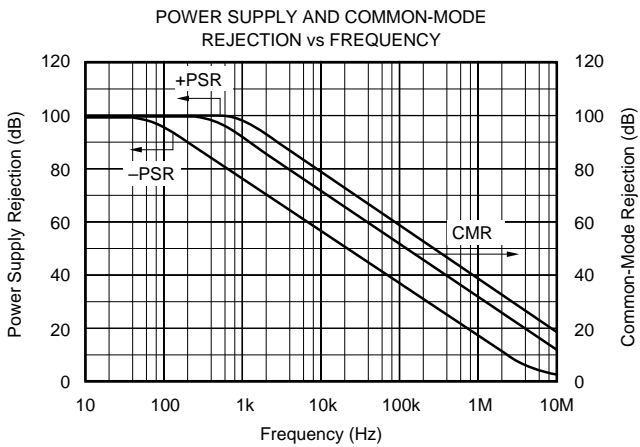
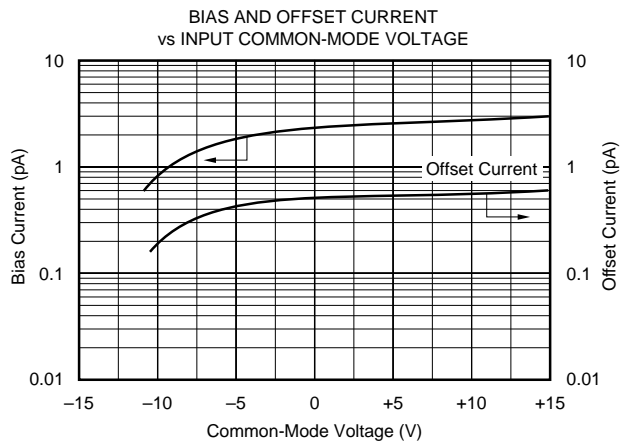
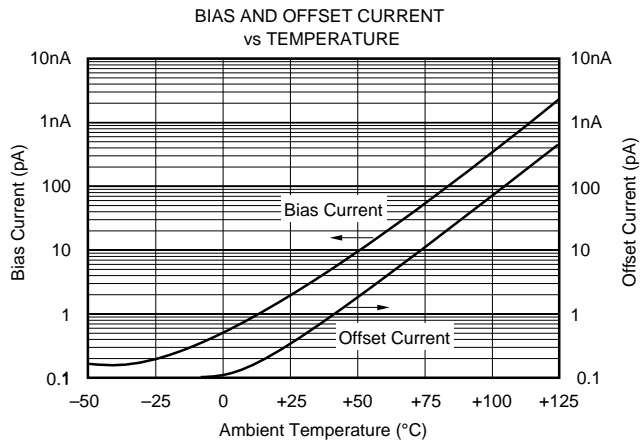
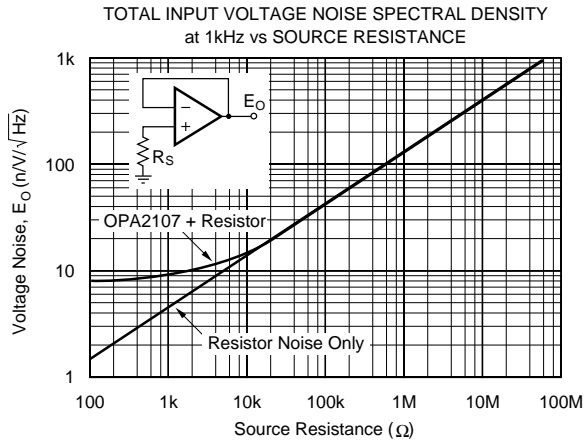
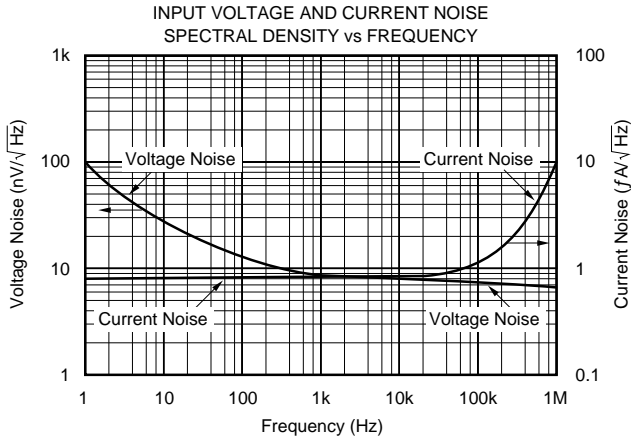
PAD	FUNCTION
1	Out A
2	-In A
3	+In A
4	$-V_S$
5	+In B
6	-In B
7	Out B
8	$+V_S$

Substrate Bias: $-V_S$

	MILS (0.001")	MILLIMETERS
Die Size	97 x 77 ± 3	2.46 x 1.96 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count		53
Backing		None

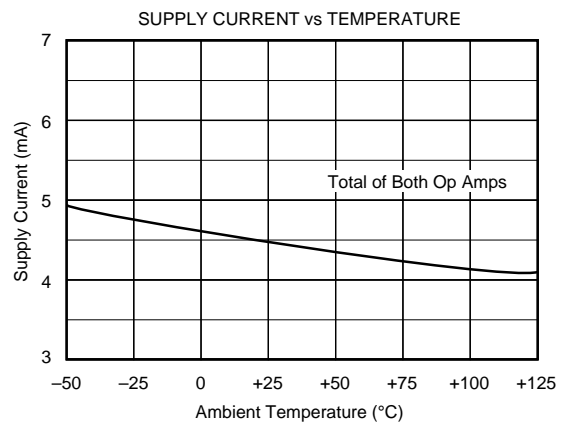
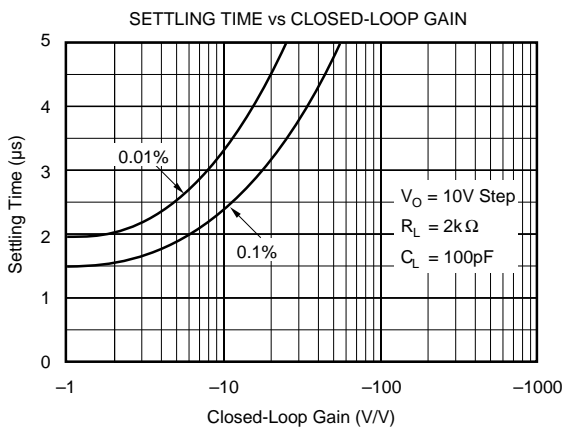
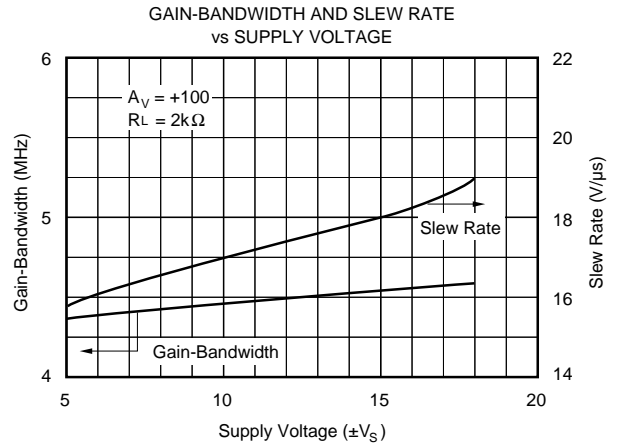
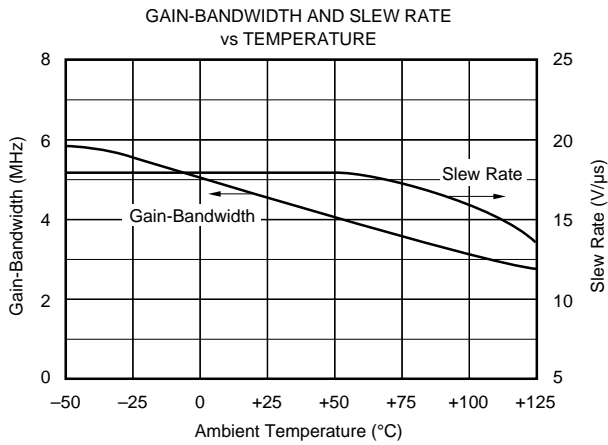
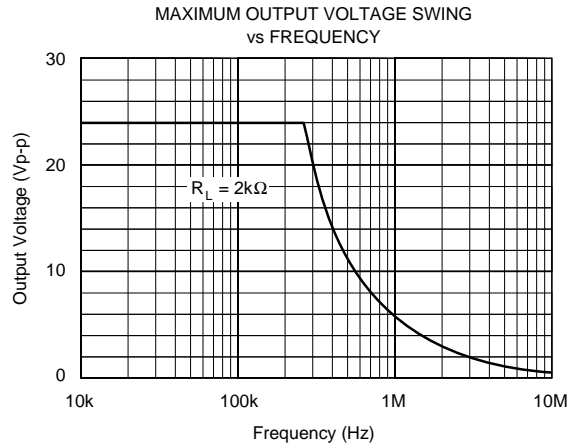
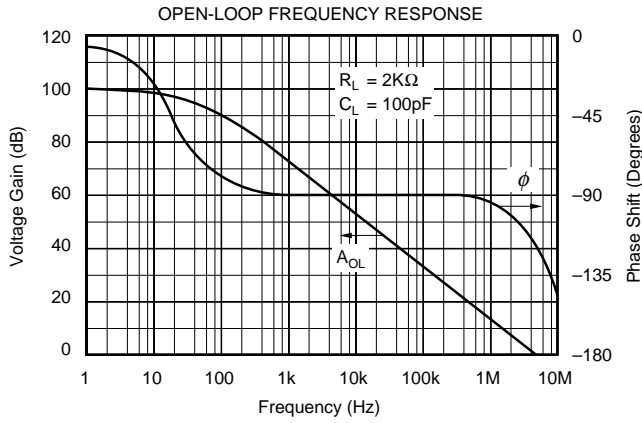
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



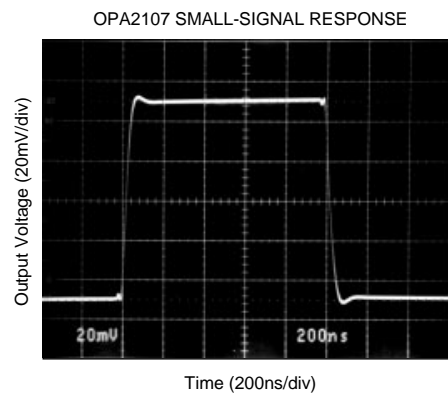
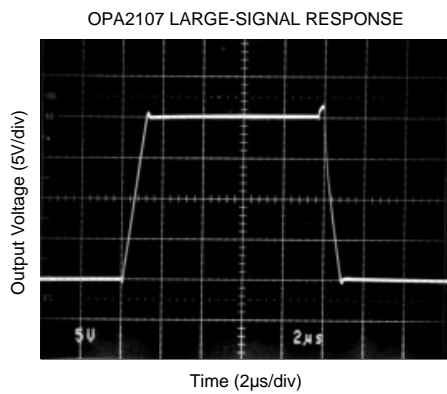
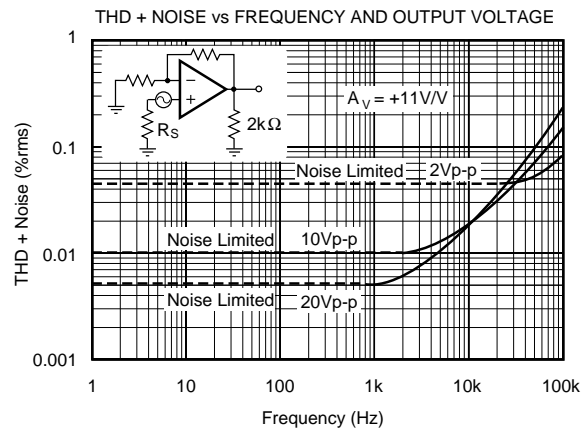
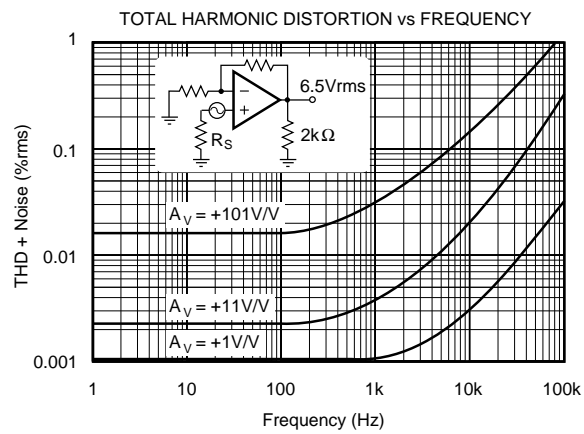
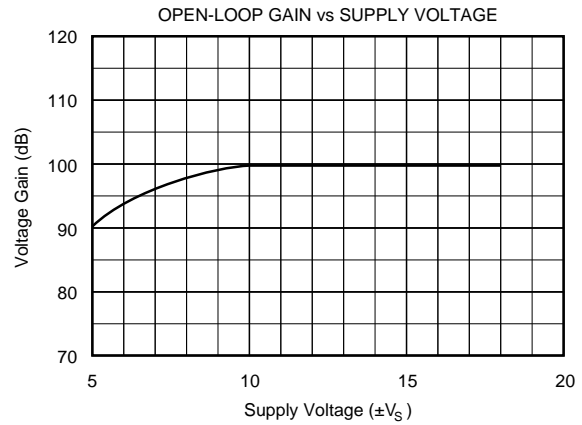
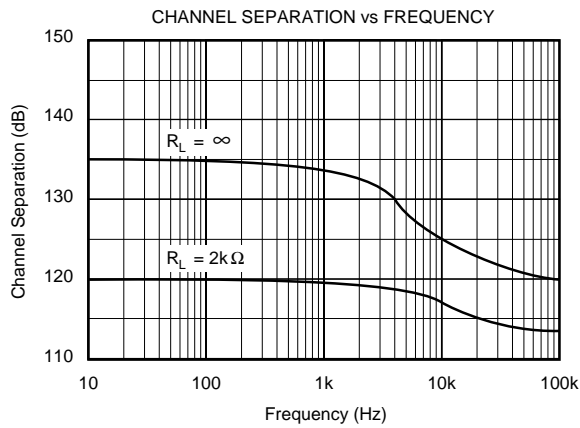
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has excellent phase margin. This makes it easy to use in a wide variety of applications.

Power supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107's *Difet* input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances a two-step cleaning process is adequate using a clean organic solvent rinse followed by de-ionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit board guard pattern effectively reduces errors due to circuit board leakage (Figure 1). By encircling critical high impedance nodes with a low impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

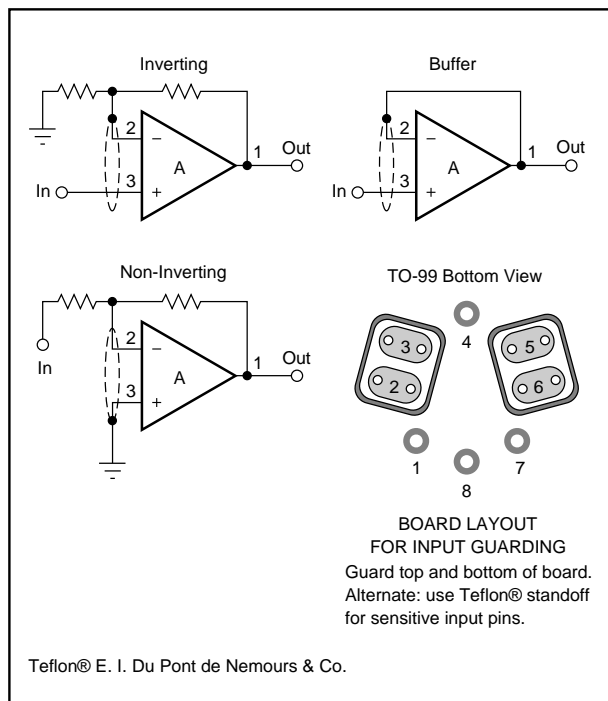


FIGURE 1. Connection of Input Guard.

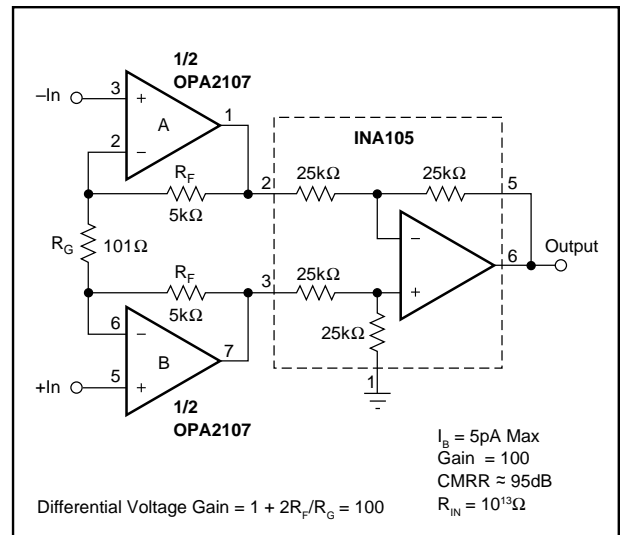


FIGURE 2. FET Input Instrumentation Amplifier.

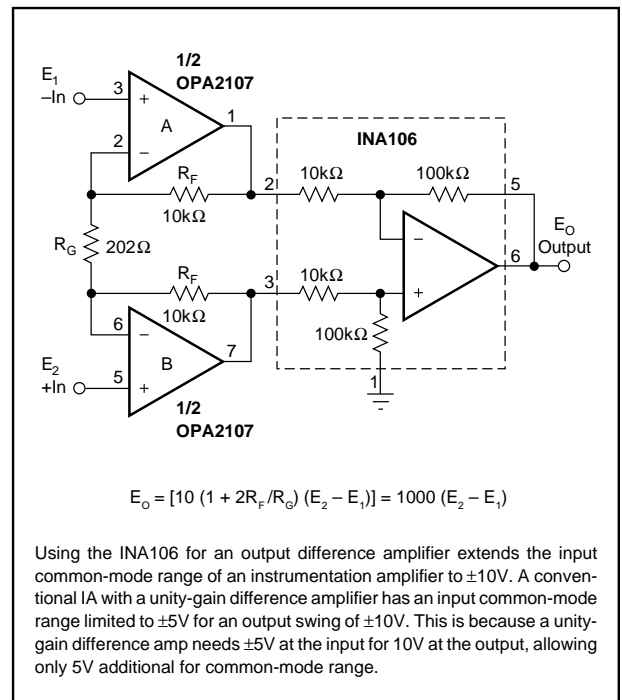


FIGURE 3. Precision Instrumentation Amplifier.

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